

Source - https:// www.javatpoint. com/number system-in-digital -electronics

## 22EC203 DIGITAL ELECTRONICS

Hours Per Week :

| L | T | P | C |
| :--- | :--- | :--- | :--- |
| 2 | 2 | 2 | 4 |

## PREREQUISITE KNOWLEDGE: Boolean algebra

## COURSE DESCRIPTION AND OBJECTIVES:

Digital Electronics deals with fundamentals Boolean Algebra and Boolean expressions that are used to realize combinational and sequential circuits. Its objective is to minimize the logical expressions using Boolean postulates and K-maps, and to design various combinational and sequential circuits and to provide with sufficient number of applications.

## MODULE-1

## UNIT-1

$6 L+6 T+6 P=18$ Hours

## BASICS OF LOGIC FUNCTIONS AND SIMPLIFICATIONS:

Switching Functions: Canonical and Standard Forms - SOP and POS forms, Logic Gates: Logic gates, Algebraic simplification and realization with basic gates and universal gates, Simplification of logic functions: Karnaugh maps - 3, 4, 5 variables.

## UNIT-2

10L+10T+10P=30 Hours

## COMBINATIONAL LOGIC DESIGN:

Combinational Logic Design Part I: Design using conventional logic gates, Half adder, Full adder, Half Subtractor, Full Subtractor, Ripple carry adder, Adder/Subtractor, BCD adder, Code converters, Comparator, Parity generator/detector.

Combinational Logic Design Part II: Decoder, Encoder, Multiplexer, De-multiplexer, Design of combinational circuits using multiplexer and decoder.

## PRACTICES:

Design and Implementation of

- Basic Logic Gates.
- Adders: Half Adder, Full Adder, Ripple carry adder, Adder/Subtractor, BCD adder
- Subtractors: Half Subtractors, Full Subtractors.
- Encoder \& Decoder.
- Multiplexer \& De-Multiplexer.
- Parity Circuits.
- Code Converters.
- Comparator

MODULE-2

## UNIT-1

$6 L+6 T+6 P=18$ Hours

## SEQUENTIAL DESIGN:

Sequential Logic Design Part I: Classification of sequential circuits, Latches, Flip-Flops - SR, JK, D, T, Master slave flip flop, Triggering and excitation tables

## UNIT-2

10L+10T+10P=30 Hours

## ASYNCHRONOUS \& SYNCHRONOUS CIRCUITS:

Sequential Logic Design Part II: Shift registers, Counters - Ripple counters, Mod-n counter. Finite State Machines: State diagram, State table, Design of sequential counter, Mealy FSM, Moore FSM, Case study: Sequence Detectors, Traffic light control system.

## PRACTICES:

Design and Implementation of

- Flip Flops: SR, JK, D, T.
- Registers.
- Counters.
- Sequence Detectors

COURSE OUTCOMES:
Upon successful completion of this course, students will have the ability to:

| CO <br> No. | Course Outcomes | Blooms <br> Level | Module <br> No. | Mapping <br> with POs |
| :---: | :--- | :---: | :---: | :---: |
| 1 | Apply the knowledge of digital logic concepts to <br> optimize digital circuits.. | Apply | 1 | $1,2,4,5,9$, <br> 10,12 |
| 2 | Develop Combinational digital circuits for given <br> problem statement by applying the digital tech- <br> niques. | Apply | 1 | $1,2,5,9,10$ |
| 3 | Analyze sequential digital circuits for given prob- <br> lem statement | Analyze | 2 | $1,2,3,5,9$, <br> 10 |
| 4 | Design a given application using Finite State <br> machines | Analyze | 2 | $1,2,5,9,10$, <br> 12 |

## TEXT BOOKS:

1. M. Morris Mano, "Digital Design", 6th Edition, Pearson Education, 2018.
2. ZviKohavi, Niraj K. Jha, "Switching and Finite Automata Theory", 3rd Edition, Cambridge University Press, 2009.

## REFERENCE BOOKS:

1. John.M Yarbrough, "Digital Logic Applications and Design", Thomson Learning, 2006.
2. Charles H.Roth. "Fundamentals of Logic Design", 6th Edition, Thomson Learning, 2013.
3. Donald P.Leach and Albert Paul Malvino, "Digital Principles and Applications", 6th Edition, TMH, 2006.

## SKILLS:

$\checkmark$ Minimize the logic functions using Boolean Algebra/K-map
$\checkmark$ Identify the different gates and their properties.
$\checkmark$ Design combinational and sequential circuits for a given application.

